

RHEiMS Rapid Hierarchical Energy Investigation and Modeling System

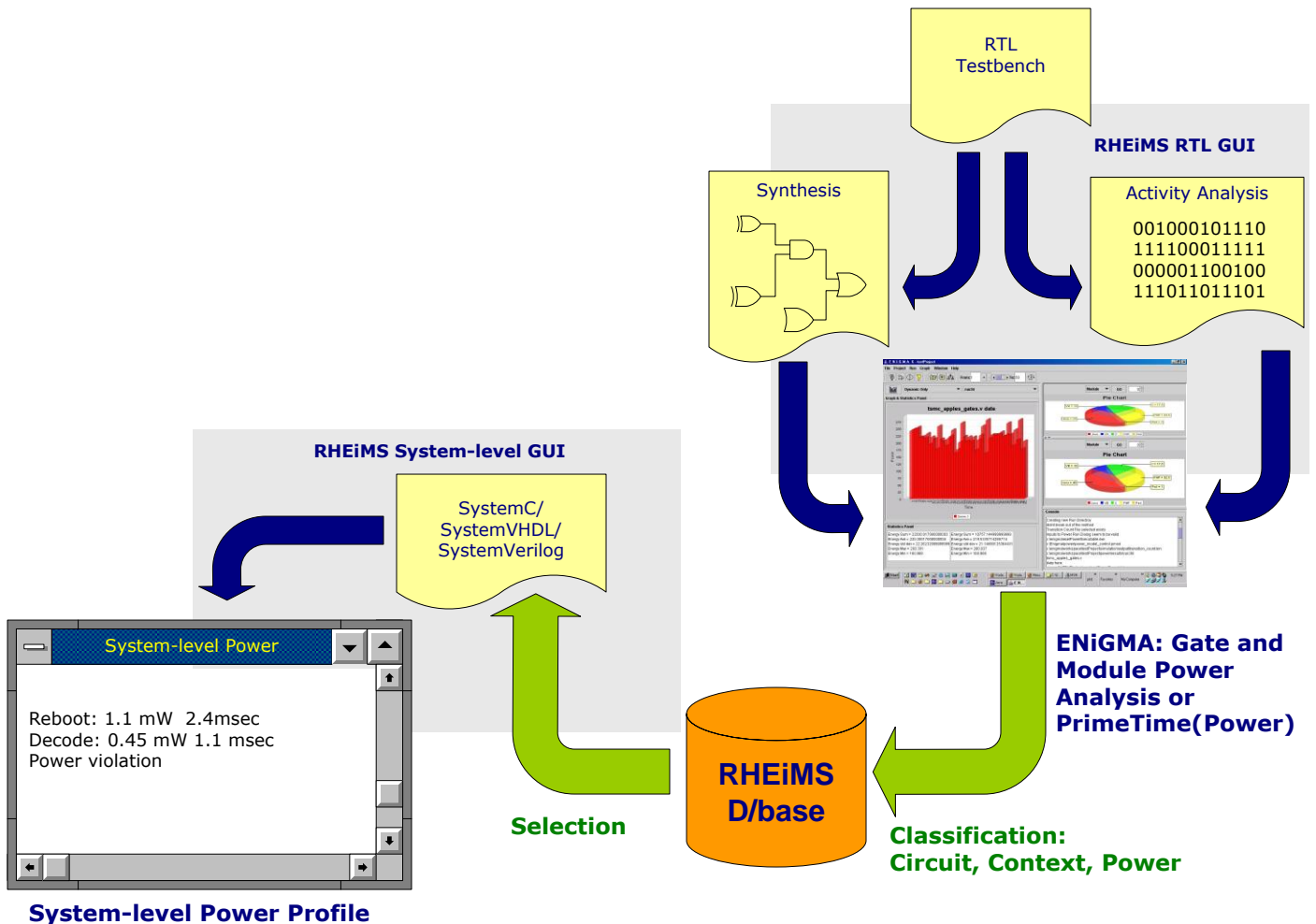
RHEiMS is a System-level Case Based power exploration tool, that delivers rapid and accurate power assessment on System level prototypes written in SystemC, SystemVerilog or SystemVHDL. RHEiMS provides a conduit for the detailed power information gathered from successive synthesised designs, to be presented in an intuitive, informative and customisable format that can be used within the context of System-level design tools.

Consequently, while a design is still at a conceptual, embryonic stage of development, the following options are open to the designer:

- **Accurate power assessment** in a Timed or Un-timed Transactional-level domain **3 orders of magnitude faster** **And within 1.5% accuracy of gate-level power estimation.**
- Power analysis of **Embedded Code driven** systems.
- **Rapid prototyping** of various architectures that can **reduce a circuit's power consumption by up to 75%.**

In RHEiMS a synergy is generated between the testbench and system-level phases in a normal design flow. The input/output behaviour and the synthesised RTL code of various components and operations are **Classified** through the **RHEiMS RTL GUI** to produce **Cases** that are stored in the **RHEiMS Database** for subsequent **Selection** and use by the **RHEiMS System-level Design Entry GUI**. Associated with each case is a parameterisable system-level power model that can be customised to the specific circumstances and use of the component in the system-level design.

The detailed cycle accurate power analysis required for the generation of comprehensive system-level power models is provided by Neosera's **ENiGMA** (ENergy Investigation via Gate and Module Analysis) power analysis acceleration processor. This rapidly delivers dynamic and leakage power information at gate and module level that may also be used for RTL power assessment. Alternatively, any proprietary gate-level power estimation tool such as **Synopsys' PrimeTime(Power)** can be used to generate the power models.



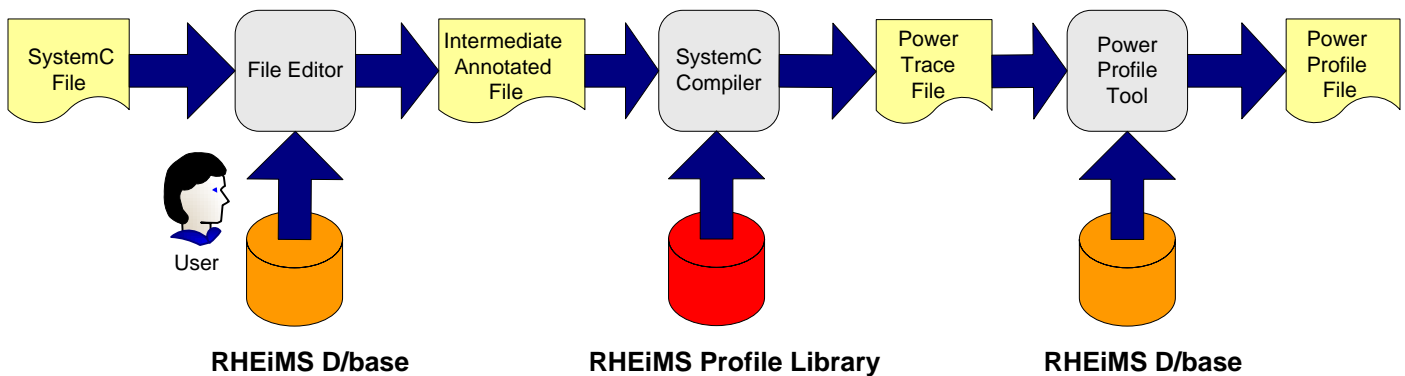
THE RHEiMS System-level Power Analysis Tool

The classification process in RHEiMS enables the system-level engineer to browse and identify key components, and their operational context or mode of operation. From an extensive database of previous designs, the system-level code is annotated with selected cases. Execution of the annotated code with the **RHEiMS library** generates system-level power analysis data.

The RHEiMS RTL GUI provides a user-defined classification mechanism that automatically augments the database with details of each new component, the context in which it is used and the details of its power consumption. RHEiMS introduces the concept of **Experiential Design**, the invaluable experience and knowledge gained in previous designs is used to guide and inform the development of the new.

The System-level GUI

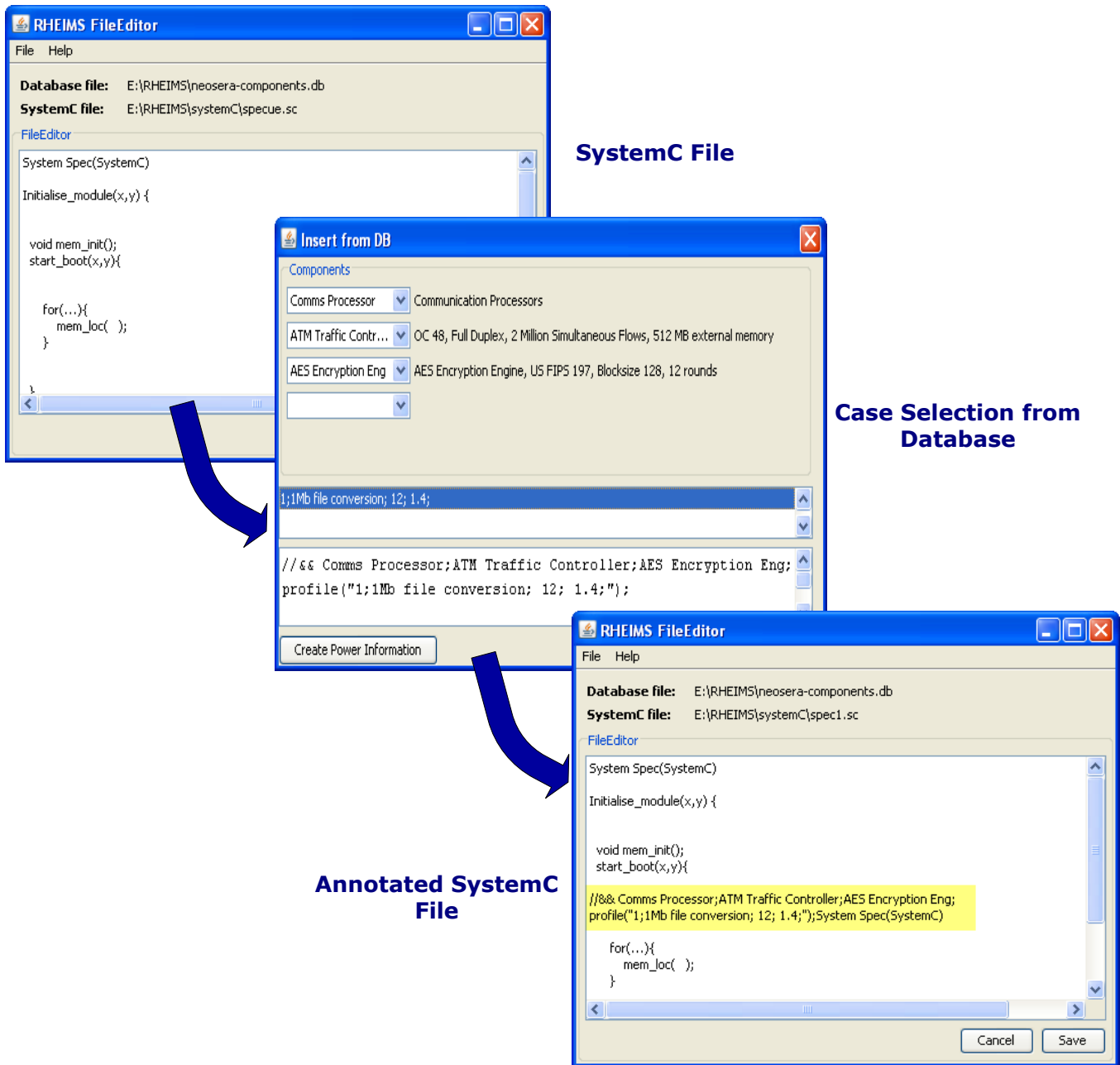
The RHEiMS system-level GUI operates with system-level (Transactional) languages such as SystemC, SystemVerilog and SystemVHDL. The System engineer can investigate and query the RHEiMS database containing all the classified cases generated from previous designs and simulation runs. The system-level code is **annotated** with the various designer-selected choices from the database. The behaviour of the annotated file is identical to that of the original file except that additionally a power profile can be generated from the trace file using the RHEiMS Power Profiler tool and database. Each prototype design represents a particular implementation of the source Transaction-level file in terms of primitive blocks and actions (Cases) that can be saved as an annotated file.



The RHEiMS system provides an adaptable and comprehensive power modelling capability with customisable conditions:

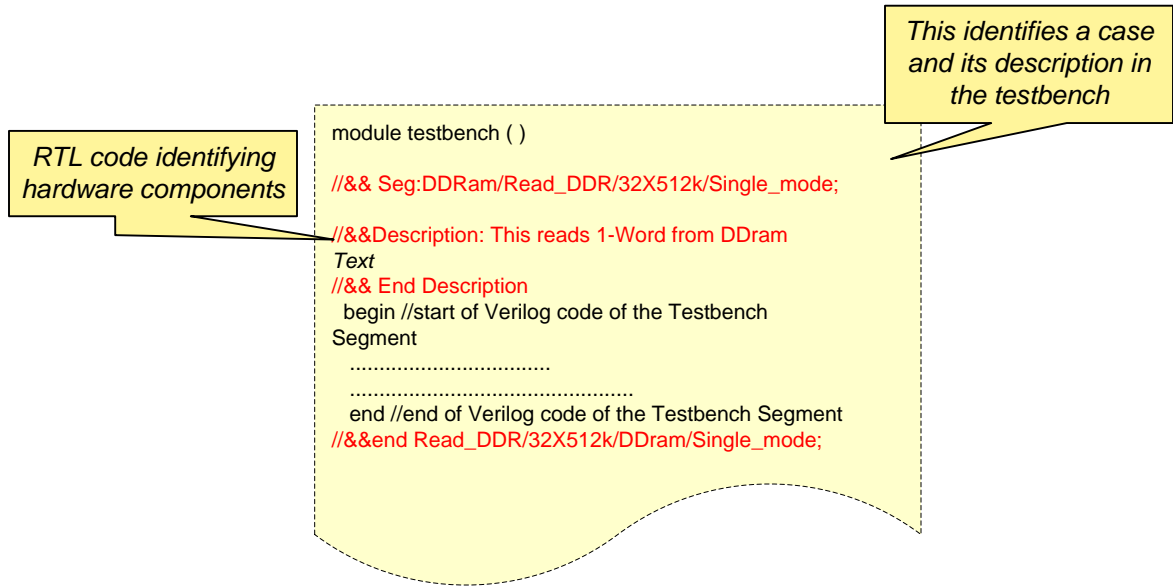
- **Static Cases** in which the power consumption of associated component and action is not data dependent.
- **Dynamic Cases** in which the power consumption is data dependent and the data stream is specified in a file or memory structure.
- Alternative operational conditions such as **frequency** and **voltage** can be specified for each case.

The System-level Annotating(Case Selection) Interface



The System-level RTL-level Interface

This interface provides an easy and intuitive method of annotating an existing design, to define cases for which RHEiMS will subsequently generate power models.

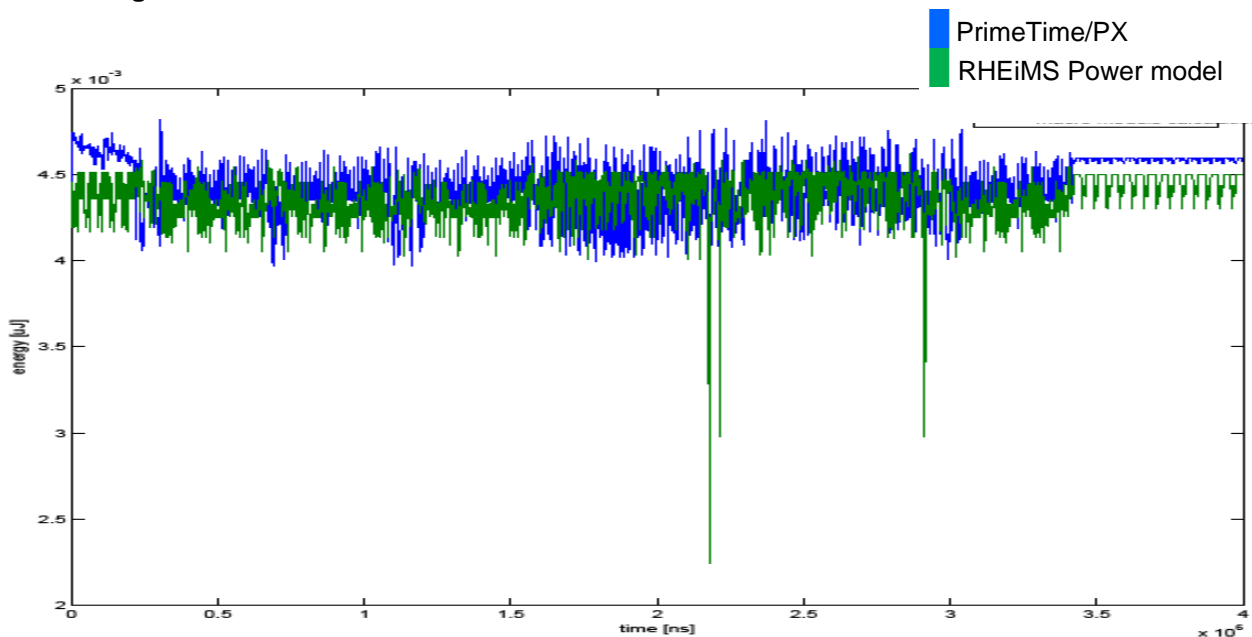


Accuracy and Speed Performance of RHEiMS versus A Gate-level Power analysis Tool (PrimeTime/PX)

The following benchmarks were generated using a Sort and Square-root algorithm executing on a 8051 processor. This equated to the execution of 4030 and 3623 instructions, representing 3.6ms and 3.42 ms of actual processing time respectively. The 8051 was synthesised using the TSMC .13 library.

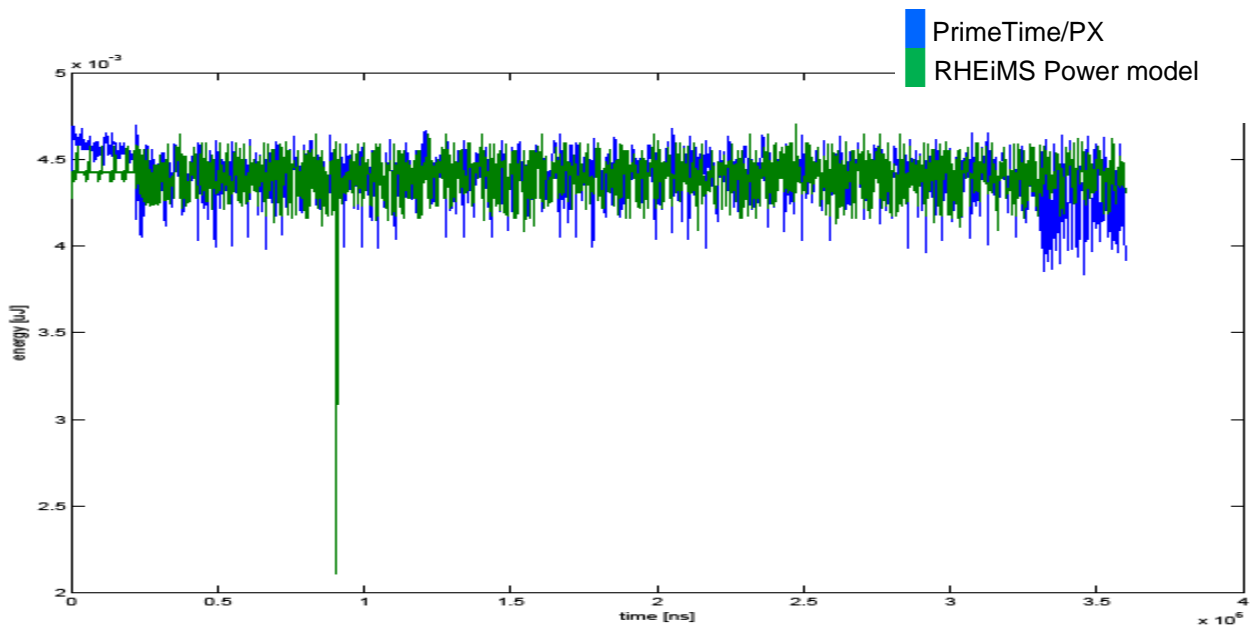
Power consumption was determined using PrimeTime/PX with the benchmarks and compared to the same benchmarks executing on a 8051RHEiMS power model. The power model was generated from an independent, alternative set of operating conditions using data produced by PrimeTime. The once-off production of the power model took approximately 18.75 of CPU time to produce. This could be substantially reduced (approximately by a factor 10) by use of Neosera's ENiGMA tool.

Square-root Algorithm on 8051



Normal System-level simulation (C-code) of 8051 executing square-root application	4.125 sec
System-level simulation of 8051 + generation of data required by RHEiMS power model	16.156 sec
Execution time of PrimeTime/PX	17.6 hrs (6.34 X 10 ⁴ sec)
Execution time of RHEiMS	83.7 sec
Speedup (PrimeTimePX exec- time/RHEiMS exec- time)	757
Power estimation PrimeTime/PX	6.33 mW
Power estimation RHEiMS	6.34 mW
RHEiMS accuracy (w.r.t PrimeTime/PX)	99.84%

SORT Algorithm on 8051



Normal System-level simulation (C-code) of 8051 executing square-root application	5.312 sec
System-level simulation of 8051 + generation of data required by RHEiMS power model	15.765 sec
Execution time of PrimeTime/PX	19.8 hrs (7.13×10^4 sec)
Execution time of RHEiMS	92.79 sec
Speedup (PrimeTimePX exec- time/RHEiMS exec-time)	768
Power estimation PrimeTime/PX	7.08 mW
Power estimation RHEiMS	6.98 mW
RHEiMS accuracy (w.r.t PrimeTime/PX)	98.64%

RHEiMS Value Proposition

- Power reduction up to 75% in designs through the novel experiential design concept.
- System-level Embedded code driven power analysis.
- A intuitive and easy to use system-level power analysis tool.
- A shorter design cycle through faster optimal design selection.
- Three orders of magnitude faster but within 1.5% accuracy of gate-level power estimation.